

LAW OFFICES
McGuireWoods LLP
1750 TYSONS BOULEVARD, SUITE 1800
MCLEAN, VIRGINIA 22102

APPLICATION
FOR
UNITED STATES
LETTERS PATENT

Applicants: Dureseti Chidambarao, Omer H. Dokumaci
and Oleg G. Gluschenkov
For: IMPROVED NFETs USING GATE
INDUCED STRESS MODULATION
Docket No.: FIS920030186US1

IMPROVED NFETs USING GATE INDUCED STRESS MODULATION

BACKGROUND OF THE INVENTION

Field of Invention

The invention generally relates to methods for manufacturing a semiconductor device with improved device performance, and more particularly to methods for manufacturing semiconductor devices which impose tensile and compressive stresses in the substrate of the device during device fabrication.

Background Description

Mechanical stresses within a semiconductor device substrate can modulate device performance. That is, stresses within a semiconductor device are known to enhance semiconductor device characteristics. Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses are created in the channel of the n-type devices, e.g., NFETs and/or p-type devices, e.g., PFETs. However, the same stress component, either tensile stress or compressive stress, discriminatively affects the characteristics of an n-type device and a p-type device.

In order to maximize the performance of both NFETs and PFETs within integrated circuit (IC) chips, the stress components should be engineered and applied differently for NFETs and PFETs. That is, because the type of stress which is beneficial for the performance of an NFET is generally disadvantageous for the performance of the PFET. More particularly, when a device is in tension (in the direction of current flow in a planar device), the performance characteristics of the NFET are enhanced while the

performance characteristics of the PFET are diminished. To selectively create tensile stress in an NFET and compressive stress in a PFET, distinctive processes and different combinations of materials are used.

For example, a trench isolation structure has been proposed for forming the appropriate stresses in the NFETs and PFETs, respectively. When this method is used, the isolation region for the NFET device contain a first isolation material which applies a first type of mechanical stress on the NFET device in a longitudinal direction (parallel to the direction of current flow) and in a transverse direction (perpendicular to the direction of current flow). Further, a first isolation region and a second isolation region are provided for the PFET and each of the isolation regions of the PFET device applies a unique mechanical stress on the PFET device in the transverse and longitudinal direction.

Alternatively, liners on gate sidewalls, have been proposed to selectively induce the appropriate strain in the channels of the FET devices (see Ootsuka et al., IEDM 2000, p.575, for example). By providing liners, the appropriate stress is applied closer to the device than the stress applied as a result of the trench isolation fill technique.

While these methods do provide structures that have tensile stresses being applied to the NFET device and compressive stresses being applied along the longitudinal direction of the PFET device, they may require additional materials and/or more complex processing, and thus, resulting in higher cost. In addition, in the methods described above, for example, the stresses in the channel are relatively moderate (i.e., for example, about 200 to about 300 MPa), which provide approximately a 10% benefit in device performance. Thus, it is desired to provide more cost-effective and simplified methods for creating stronger tensile and compressive stresses in the channels NFETs and PFETs,

respectively. It is further desired to create larger tensile stresses in the channels of the NFETs than the tensile stresses created as a result of the known processes described above.

SUMMARY OF THE INVENTION

In a first aspect, this invention provides a method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor by covering the p-type field effect transistor with a mask. A portion of a gate polysilicon of the n-type field effect transistor is oxidized such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor.

In a second aspect, this invention separately provides a method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor on a semiconductor wafer by oxidizing a portion of a gate polysilicon of the n-type field effect transistor, such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type field effect transistor.

In a third aspect, this invention separately provides an integrated circuit, including: a p-type transistor having a polysilicon layer and an n-type transistor having a polysilicon layer, wherein, after oxidation of the polysilicon layer of the n-type transistor,

the polysilicon layer of the n-type transistor has an oxide edge with the shape of a vertical bird's beak.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts desired stress states for PFETs and NFETs;

Figures 2(a) through 2(k) depict a process for forming gate MOSFETs according to the invention;

Figures 3(a) through 3(g) depict a portion of another process for forming gate MOSFETs according to the invention;

Figure 4 depicts stresses in a silicon structure after oxidation of the gate polysilicon according to the invention; and

Figure 5 depicts stresses in a silicon structure after etching of deposited oxide during oxidation of the gate polysilicon according to the invention.

DETAILED DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

The invention provides a method for fabricating devices with improved performance characteristics. In this invention, oxidation of the gate polysilicon is used to control the stresses in complimentary metal oxide semiconductor (CMOS) NFET devices such that their performances are enhanced without degrading the performance of the PFET devices.

In one aspect of the invention, polysilicon of an NFET gate is oxidized while the polysilicon of a PFET gate is masked to prevent the polysilicon of the PFET from being oxidized. By preventing the oxidation of the polysilicon of the PFET, degradation of hole mobility is prevented. In this aspect, the oxidation of NFET gates creates tensile stresses in the channels of the NFETs without creating tensile stresses in the channel of the PFETs. By oxidizing the gate polysilicon of the NFETs large stresses of about 500MPa to about 1000MPa, for example, are formed in a channel of the NFET. In one implementation the stresses are about 700MPa. By providing tensile stresses to the channel of the NFET without providing tensile stresses in the channel of PFET, the charge mobility and drive current along the channels of the NFET devices are enhanced without diminishing the charge mobility and drive current along the channels of the PFET devices.

By implementing the stresses using a polysilicon over-etch, this invention provides the implementation of stresses which are self-aligned to the gate, whereas in the isolation induced stress structures, the stresses are not self aligned to the gate. This invention also provides stress levels in the silicon under the gate which are much larger than the isolation-based or liner-based approaches.

Also, when gates that are confined by oxide fill are used, the expansion of the oxide in the gate stack is relatively confined. Further, when a confined gate is subjected to oxidation, the gate channel is put under tension. The gate is put under tension because oxide deposited thereon expands outwardly at the top. This results in compression in the top part of the isolation. At the same time, by inducing bending stresses at the bottom part of the isolation, next to the polysilicon under tension, the channel receives large

tensile stresses. These stress levels are on the order of about 500 to about 1000 MPa and these tensile stresses are beneficial to the NFET drive currents. In this invention, the PFETs are masked during oxidation of the NFETs so that the creation of tensile stresses from this oxidation step in the PFETs is substantially and/or completely prevented in order to not diminish the performance of the PFET. Thus, the invention provides for tensile stresses along the channel of the NFETs without providing tensile stresses along the channels of the PFETs to improve the performance of the NFET devices without diminishing the performance of the PFET devices.

Figure 1 illustrates desired stress states for improving the performance of PFETs and NFETs (see Wang et al, IEEE Trans. Electron Dev., v.50, p.529, 2003). In Figure 1, an NFET and a PFET are shown to have a source region, a gate region and a drain region. The NFET and PFET are shown to have arrows extending outward from the active area to illustrate tensile stresses. The arrows extending inward toward the PFET device are illustrative of compressive forces. More specifically, the outwardly extending arrows, shown extending from the NFET, illustrate a tensile stress that is desired in the transverse and longitudinal directions of the device. Similarly, the inwardly extending arrows, shown with relation to the PFET, illustrate a desired longitudinal compressive stress. The range of stresses needed to influence device drive currents is typically on the order of a few hundred MPa to a few GPa. The width and the length of the active area of each device is represented by "W" and "L", respectively. It should be understood that each of the longitudinal or transverse stress components can be individually tailored to provide the performance enhancements for both devices (i.e., the NFET and the PFET).

Figures 2(a) through 2(j) depict a general exemplary process for forming the MOSFETs according to this invention. Figures 2(a) through 2(d) explain processes that are known, and thus any known applicable processes may be used. Figure 2(a) illustrates the structure after shallow trenches 5 (STI) are formed. A SOI (silicon-on-insulator) wafer which has a stack of silicon 1, buried oxide 2, and a silicon layer 3 is used. Generally, to form the STI on SOI wafers, a thin ($\sim 50\text{\AA}$) layer of silicon dioxide SiO_2 (pad oxide) (not shown) is grown on the silicon layer 3, which is on the buried oxide layer 2 on the silicon substrate 1, by reacting silicon and oxygen at high temperatures. A thin layer (about 1000\AA to about 2500\AA) of pad silicon nitride (Si_3N_4) (not shown) is then deposited using chemical vapor deposition (CVD). Next, the patterned photoresist with a thickness of about 0.5 to about 1.0 microns is deposited, and the structure is exposed and developed to define the trench areas 5. Next, the exposed SiO_2 and the Si_3N_4 are etched using reactive ion etching (RIE). Next, an oxygen plasma is used to burn off the photoresist layer. A wet etch is used to remove the pad Si_3N_4 and pad oxide. Then, an oxide layer is deposited to fill the trenches and the surface oxide is removed using chemical mechanical polishing (CMP). This completes the formation of STI as seen in Figure 2(a).

Next, a sacrificial oxide (not shown) of about 50\AA is grown on the silicon. Then, as shown in Figure 2(b) an n-well 10 and a p-well 12 are formed. Patterned photoresist layers are used to successively form the n-well 10 (using, for example, multiple implants of Phosphorous ions) and the p-well 12 (using, for example, multiple implants of Boron ions). The well implants 10 and 12 are then optionally annealed. The sacrificial oxide

layer is then removed using a wet HF solution, such that a clean silicon surface is left behind.

Next, as shown in Figure 2(b), a gate oxide layer 14 of about 10Å to about 100Å is grown. On the gate oxide layer 14, a polysilicon layer 16 is deposited using CVD to a thickness of about 500Å to about 1500Å to form the gate electrodes 18 and 20 shown in Figure 2(c). Patterned photoresist layers (not shown) are used to define the gate electrodes. RIE is used to etch the exposed portions of the polysilicon layer 16 and the photoresist patterns are stripped away in order to complete formation of the gate stack of the n-type transistor 17 and the gate stack of the p-type transistor 19.

Figure 2(c) shows the formed gate electrodes 18 and 20. A thin layer of oxide 15 is then grown on the remaining polysilicon. Patterned photoresist layers (not shown), which are later removed, are used to successively tip (and halo countering doping implants) implant the n-type and p-type transistors. For n-type transistors, a very shallow and low dose implant of arsenic ions, for example, may be used to form the p-tip 22 (while a Boron implant, for example, may be used for halos). For p-type transistors, a very shallow and low dose implant of BF₂ ions, for example, may be used to form n-tip 24 (while an arsenic implant may, for example, be used for halos).

Still referring to Figure 2(c), spacers 26 are formed by depositing a silicon nitride layer (not shown) using CVD to a thickness of about 100Å to about 1000Å and then etching the nitride from the regions other than the sidewalls of the gate. Patterned photoresist layers (not shown), which are removed prior to the next stage of the process, are used to successively create the source/drain regions of the transistors.

In Figure 2(d), for the n-type transistors, a shallow and high-dose of arsenic ions, for example, may be used to form the source/drain regions 28 while the p-type transistors are covered with the corresponding photoresist layer. For the p-type transistors, a shallow and high dose of BF_2 ions, for example, may be used to form the source/drain regions 30 while the n-type transistors are covered with the corresponding photoresist layer. An anneal is then used to activate the implants. The exposed oxide on the structure is then stripped by dipping the structure in HF in order to expose bare silicon in the source, gate and drain regions of the transistors.

Still referring to Figure 2(d), metal or a low resistance material 32 is deposited to a thickness of about 30\AA to about 200\AA across the wafer surface in order to form silicide. The silicide could be formed from reacting the underlying with any deposited metal such as Co, Hf, Mo, Ni, Pd, Pt, Ta, Ti, W, and Zr. In the regions, such as, the source, drain and gate regions, where the deposited metal is in contact with silicon, the deposited metal or low resistance material reacts with the silicon to form silicide. In the other regions (i.e., where the deposited metal is not in contact with silicon), the deposited metal remains unchanged. This process aligns the silicide to the exposed silicon and is called “self-aligned silicide” or salicide.

The unreacted metal is then removed using a wet etch while the formed silicide 34 remains, as shown in Figure 2(e). As shown in Figure 2(e), an oxide fill followed by chemical mechanical polishing is used to planarize the surface. CMP is used to make the oxide fill flat and such that the oxide fill is flushed with the top of the gates. Next, as shown in Figure 2(f), the silicide 34 on top of the polysilicon is removed using a selective etch.

In methods according to the invention, the PFET devices of the structure shown in Figure 2(g) are masked, using a mask 38. The mask 38 may be, for example, a hard mask, such as for example, a mask made of nitride. To form the mask 38, nitride, for example, may be deposited on the silicon wafer and the nitride covering the polysilicon gates of the NFETs may be etched to expose the polysilicon gates of the NFETs. The mask exposes the NFETs so that the additional silicide 34 on the gate polysilicon of the NFETs may be etched off from the gate polysilicon of the NFET, as shown in Figure 2(g).

As shown in Figure 2(h), the mask 38 covers the PFETs during oxidation of the NFETs, such that the gate polysilicon of the PFETs is not oxidized while oxide 40 is deposited on the gate polysilicon of the NFETs.

As also shown in Figure 2(i), oxidation of the gate polysilicon of the NFETs results in the formation of a vertical bird's beak 44 in the edge of the polysilicon of the NFETs. The oxidation of the gate of the NFETs creates large tensile stresses in the channel region of the NFETs. Since the PFETs are masked, with mask 38, the polysilicon gates of the PFETs are not oxidized. Further, these tensile stresses increase electron mobility along the channel, and improve the performance of the NFETs. The oxidation of the gate polysilicon of the NFETs should be a low temperature oxidation, such as, for example, high pressure oxidation, atomic oxidation or plasma oxidation. The oxidation step should be performed at a low temperature, such as, 600°C or less in order to prevent degradation of device characteristics, via, for example, deactivation or diffusion. Low temperature oxidation should be used so that (a) the already created silicide on the source/drain regions does not agglomerate and/or change resistivity and (b)

so that the extensions, and source and drain dopants do not diffuse and/or deactivate. Typically, the oxidation should result in about a vertically formed bird's beak of about 20Å to about 100Å in width and height.

As shown in Figure 2(i), the vertical bird's beak 44 causes the base of the polysilicon to be wider than an uppermost surface of the polysilicon and the side edges of the polysilicon taper towards the uppermost surface thereof. In addition, as shown in Figure 2(i) in a region where the polysilicon tapers towards the uppermost surface, a portion of the gate stack 17 of the NFET comprises a portion of the polysilicon layer and a portion of the deposited oxide forming a vertical bird's beak 44 are present along a plane perpendicular to a plane of the base of the polysilicon. Each vertical bird's beak 44 may have, for example, a width of about 20Å to about 100Å.

As further shown in Figure 2(j), the oxide above the gate polysilicon of the NFETs is etched off while the vertical oxide bird's beak is still preserved. The stresses created in the gate polysilicon of the NFETs are maintained even after removal of this oxide on top of the polysilicon as a result of the vertical bird's beak formed in the gate polysilicon of the NFETs because of the oxidation step, as shown in Figures 4 and 5. As also shown in Figure 2(j), the mask 38 has been removed.

Then, as shown in Figure 2(k), silicide forming material 46 is deposited on the polysilicon gate of the NFETs after removing the mask 38. Material, such as, for example, Co, HF, Mo, Ni, Pd₂, Pt, Ta, Ti, W, and Zr may be used to form the silicide. When material, such as, for example, Co, HF, Mo, Ni, Pd₂, Pt, Ta, Ti, W, and Zr is deposited on silicon, the silicon reacts with the material and silicide is formed. The material for forming silicide may be deposited over the wafer via, for example,

evaporation, sputtering, or CVD techniques. Next, the structure is heated to temperature of about 300°C to about 700°C to allow the deposited silicide material to react with the polysilicon. During sintering, silicide only forms in the regions where metal is in direct contact with silicon or polysilicon. The remaining unreacted silicide material is then removed, for example, with a selective etch without damaging the formed silicide. After this, the standard middle of the line (e.g., passivation and contact formation) and back end of the line (various interconnect metal, via, and interlevel dielectrics) processes are performed.

In another embodiment of the invention, a nitride cap may be provided on the gate polysilicon of the NFET instead of the metal or low-resistance material. For ease of discussion, the portions of the process which are the same as the processes described with regard to Figures 2(a) – 2(k) will not be repeated below. In this embodiment, the description of the structure illustrated in Figures 2(a) and 2(b) applies to the structure illustrated in Figures 3(a) and 3(b). Then, as shown in Figure 3(c), a nitride layer 17 is deposited on the surface. As shown in Figure 3(d), spacers 26 are formed by depositing a silicon nitride layer using CVD to a thickness of about 100Å to about 1800Å and then etching the nitride from the regions other than the sidewalls of the gate. The nitride cap 19, above the polysilicon of the NFET and PFET is retained.

As shown in Figure 3(e), silicide forming material 32 is deposited on the surface. As discussed above, a metal or a low resistance material 32 is deposited to a thickness of about 30Å to about 200Å across the wafer surface in order to form silicide 34 (see Figure 3(f)). Silicide is formed in the source and drain regions of the transistors (i.e., where the silicide is in contact with the silicon) and the unreacted material is removed. As shown in

Figure 3(g), an oxide fill 36 followed by chemical mechanical polishing is used to planarize the surface. CMP is used to make the oxide fill flat and such that the oxide fill is flushed with the top of the gates.

Next, in this embodiment, the nitride caps 19 are stripped off from the polysilicon gates of the transistors. In methods according to the invention, the PFET devices of the structure shown in Figure 3(g) are masked, using a mask 38. The description of Figures 2(g) through 2(k) applies for the remainder of the process.

Figure 4 shows the stresses in the gate structure after oxidation of the gate polysilicon of the NFET. The dashed lines represent tensile stress and the solid lines represent compressive stress. As can be seen from Figure 4, tensile stresses are present in the channel area of the NFET. In structure illustrated in Figure 4, tensile stresses of about 1GPa and less are present in the channel area of the NFET.

Figure 5 shows the stresses in the gate structure when the oxide above the gate polysilicon is etched in accordance with this invention. This etch is needed since the gate polysilicon has to be silicided for contact formation later. Similar to Figure 4, the dashed lines represent the tensile stress and the solid lines represent the compressive stress. As can be seen from Figure 5, the stresses in the NFET device is maintained even after etching of the oxide from above the gate polysilicon.

The tensile stresses in the NFET device is maintained even after etching of the oxide due to the formation of the vertical bird's beak in the gate polysilicon as a result of the oxidation of the gate polysilicon. The desired stresses are tensile and add values of the order of 200MPa and above.

By providing tensile stresses to the channel of the NFET and without creating additional tensile stresses in the channel of the PFETs, the charge mobility along the channels of NFET devices is enhanced while the hole mobility along the channels of the PFET devices is maintained. Thus, as described above, the invention provides a method for providing tensile stresses along the longitudinal direction of the channel of NFET devices by oxidizing the polysilicon gate of the NFET devices after silicidation of the gate polysilicon.

It should be understood that this invention is readily applicable to bulk or layered SiGe substrates. It should also be understood that this invention may also be used with damascene gate structures, which have been proposed for use of high k dielectric gate oxides.

While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.